Thermal Design and Optimization Methodology for Integrated Power Electronics Modules

A methodology was developed and implemented to optimize the design layout for integrated power electronics modules (IPEMs) by considering both the electrical and thermal performances. This paper is primarily focused on the thermal aspects, which were analyzed using three-dimensional (3D) computational software tools. Implementation of the design methodology resulted in a 70 percent reduction in the common mode current, a 4 percent reduction in the size of the geometric footprint, and a 7°C reduction in the maximum temperature rise for the case studied, thus, providing an increase in the IPEM’s overall performance. [DOI: 10.1115/1.1849233]

Keywords: Integrated Design Optimization, Integrated Power Electronic Module, Thermal Analysis

1 Introduction

While thermal management is a key enabling technology for the next generation of power electronics, thermal design has evolved into an earlier stage of the product design cycle to reduce any thermal associated risk to the product. The design of power electronics involves both electrical and thermal design. Any design layout changes will not only affect the performance of the power electronics electrically but also thermally. Many design tools are available for electrical and thermal analyses. However, the tools are not integrated and, thus, electrical analysis and thermal analysis are conducted individually. Therefore, desired software tools were integrated for further improving the design process. To illustrate the integrated design methodology, a new generation of an integrated power electronic module (IPEM) was used as the design target of this research work.

An IPEM is packaged using embedded power technology—a hybrid multichip-module (MCM) based packaging technology [1]. The multiple bare chips of the metal oxide semiconductor field effect transistor (MOSFETs) or the insulated gate bipolar transistors (IGBTs) are buried in a ceramic frame, and covered by dielectrics with holes on the aluminum pads of the chips. The power devices are interconnected to other circuits by metal deposition. This new packaging method differs from the currently used technology in that the new generation eliminates wire bonds, which could lead to potential benefits from both the electrical, thermal, and reliability perspectives. The objective for this research effort was to develop and implement an integrated design strategy to improve the layout design of the IPEM by reducing the electrical stress, the conduction electromagnetic interference (EMI), and the thermal resistance, while minimizing the geometric footprint.

Parasitic inductance is a measure of the tendency for a device to store energy as the current flows through it. When a device is turned off, the energy is released as a voltage spike if no external snubber exists. The spike is a function of the inductance and the current rate, and the current rate becomes larger at higher frequencies. To improve long-term reliability, it is required that the parasitic be small enough to minimize the spike. Also the common mode capacitance must be low enough to satisfy EMI standards. Therefore, it is important to calculate both the parasitic inductance and the capacitance of the IPEM in the design process.

Thermal management is another critical task in the design of power electronic systems. Bar-Cohen [2] noted that the choice of the strategy used for the thermal management of an electronic product has a large impact on the cost, reliability, operating environment, and performance of the system. Because thermal control is one of several factors dictating enabling packaging technologies, it deserves and must receive special attention. Good thermal design is often required to achieve high reliability, low manufacturing costs, small size, and a predictable development time. Thermal and flow software simulations were used to identify hot spots and other thermally important areas on the IPEM. Assessments were made on the thermal impact of proposed design changes such as in the choice of materials and the geometric layout.

Within the module, heat is transferred primarily by conduction through numerous complex components with different thermophysical properties and thicknesses [3]. In a recent investigation of package structure optimization, researchers at the Toshiba Corporation [4] studied the temperature rise of the device as a function of the thickness of the copper base plate and metal matrix composite (MMC) base plate. They found that the effect of the thermal diffusion was large in the copper base plate compared to MMC base plate. Consequently, it decreased the temperature rise of a heat sink and the contact section. The Motorola Hybrid Power Modules Operations team [5] also studied the thermal characterization of direct bonded copper (DBC) and MCM stacks for power modules. Their results indicated that reducing the ceramic thickness would improve the maximum junction temperature with aluminum oxide (Al₂O₃), but not with aluminum nitride (AlN).

With this basis, the objective of this effort was to develop and implement an integrated electro-thermal design strategy for the
next generation of the IPEM. This paper is primarily focused on the thermal aspects of the design, while details of the electrical aspects are provided in [6].

Integrated Design Strategy

The design of IPEMs is enabled through integrated electrical and thermal modeling and analyses. Therefore, the desired software tools for electrical and thermal analyses were integrated to efficiently share data and automatically perform iterative design optimization analyses. The integration of the software tools included I-DEAS™ [9] for the geometric modeling and thermal analyses, MAXWELL [10] for electrical parameter extraction, and ISIGHT [11] for control and automation. Figure 1 shows the overview of the software integration system [12].

A two step integrated design strategy was employed. First, the parasitic inductance and capacitance of the existing IPEM (identified as Design A) were analyzed, and then a number of new electrically feasible layout improvements were proposed. The best of these was then selected and named Design B. The second step involved a detailed thermal parametric study of the Design B layout to further refine the design. Several factors were investigated, including the type of material and the thickness of the DBC ceramic substrate, and the thickness of the heat spreader. A sensitivity study was then performed to determine the uncertainty of the predicted temperatures at critical locations. The final design, Design C, was then based on a trade off between electrical, thermal, and practical considerations.

Electrical and Thermal Analyses

Electrical Modeling. The first step of the design methodology began with the development of a numerical model that included critical electrical components of the Design A IPEM. This model was used to extract the parasitic inductance and determine the capacitance values. Transient simulations and an EMI analysis were then performed to determine the electrical stress of device and the common mode EMI current. Based on these analyses, a number of new layouts were proposed to reduce the geometric footprint of the module, and a parametric study was conducted to determine the effects of the geometric size of the copper trace area and the DBC substrate thickness on the electrical performance. The best of these was selected and noted as Design B. Details of the electrical modeling and analyses are described in [6].

Thermal Modeling. The second step of the design strategy began with a detailed thermal analysis of both the Design A and Design B IPEMs using a commercial finite element and computational fluid dynamics (CFD) solver, I-DEAS™. This involved developing numerical models and carrying out simulations to identify hot spots as well as to predict steady-state temperature distributions throughout the modules. A parametric study was performed to determine the effects of the type and thickness of the ceramic substrate material, and the thickness of the heat spreader on the thermal performance of the IPEM. The parameters used in this analysis are shown in Table 1.

All of the simulations in the parametric study were performed using I-DEAS™. Each model included a full 3D IPEM with an optional heat spreader mounted on an aluminum heat sink. A flow channel, with dimensions of 69.5 mm (W)×123.5 mm (H)×325 mm (L), was included to provide airflow over the model. An inlet fan with a constant volumetric flow rate of 0.0094 m³/s was applied at one end of the channel, while the other end of the channel was vented to an ambient temperature of 50°C, as shown in Fig. 2(a). The area of the channel was fixed, resulting in an outlet velocity of 1.1 m/s. The top of the module was assumed to be adiabatic.

Each module had three heat sources: Two MOSFETs and a gate driver. The heat losses of the two MOSFETs were measured to be 12 W for the outside one (A) and 7 W for the innermost one (B). The hybrid gate driver only dissipated 1 W, as shown in Fig. 2(b). Due to its relatively low power loss, the gate driver was modeled as a homogeneous ceramic block with uniform heat generation. Fine grids were used for all heat dissipating surfaces. In addition, all soldered components and interfaces with thermal grease [e.g., at the interface between the heat spreader and the heat sink in Fig. 2(c)] were represented by equivalent thermal resistance values. Within the IPEM model, it was assumed that there was a conduction path from the two heat sources to the copper trace and the surrounding ceramic substrate, from the copper trace to the second DBC ceramic layer, and from the ceramic layer to the bottom copper layer. From there, it was assumed that the major heat flow paths involved conduction from the IPEM module to the (optional) heat spreader, conduction from the heat spreader to the heat sink, and convection from both the heat spreader and the heat sink to the ambient air. Another path of resistance was from the gate driver to the ceramic substrate, from the ceramic substrate to a layer of gel, and from the gel to the DBC layer. The generic thermal conductivities for all of the materials used in the models are listed in Table 2.

Sensitivity and Uncertainty Analysis. Once the parametric studies were completed, sensitivity and uncertainty studies were performed to determine the uncertainty of the various predicted temperatures in the model. The sensitivity, $X_{ij}$, of a given output variable $j$ (e.g., the junction temperature) to a given input parameter $i$ (e.g., MOSFET power loss) indicates how sensitive that output variable is to changes in that input parameter, while the measurement uncertainty, $\sigma_M$, reflects how accurately the input parameter values used in the model are known. Ideally, we would like the parameters associated with the highest sensitivity to have the lowest uncertainty, and parameters with highest uncertainty to have lowest sensitivity.

A four-step analysis strategy was employed for the uncertainty analysis. First, several critical model input parameters and output variables were identified, and are shown in Fig. 3. Note that the nominal values for Power Loss A and Power Loss B are the lowest values from the measurement. Thus, the uncertainty in the power loss measurement is in the positive direction only. The critical

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBC Ceramic Material</td>
<td>$\text{Al}_2\text{O}_3$</td>
</tr>
<tr>
<td>DBC Ceramic Thickness</td>
<td>0.38 mm</td>
</tr>
<tr>
<td>Heat Spreader Thickness</td>
<td>0 mm (none)</td>
</tr>
</tbody>
</table>
input parameters included the power losses of both MOSFETs and all of the interface conditions, including the epoxy, solder, and the thermal grease, and the critical output variables included the junction, gate, and minimum heat sink temperatures, and the average temperature of the module. The second step involved the determination of the measurement uncertainty for each of these parameters. These measurement uncertainties were estimated based on the experience and expertise of the power electronics packaging group in Virginia Tech. These values are shown in Table 3. The third step involved the determination of the sensitivity of each input parameter. Finally, the overall prediction uncertainties of the critical output variables were determined from the sensitivities and measurement uncertainties associated with each of the critical input parameters. Since this study focused only on the design of the module itself and not the heat sink design, the fluid flow and convection heat transfer parameters were not considered as the sensitivity parameters. Future studies will focus on the optimization of the heat sink and, therefore, the sensitivity and uncertainty analyses associated with the convection heat transfer parameters. Similarly, the uncertainties of material property values were not studied here because the focus of this paper is to demonstrate the use of integrated electro-thermal design strategy in designing and optimizing power electronics modules. However, similar methodology can also be used to analyze the sensitivity of the material properties.

The sensitivity coefficient for an output variable $j$ to an input parameter $i$ was defined as a dimensionless sensitivity coefficient, $X_{ij}$. 

Table 2 Generic thermal conductivity values at 300 K for materials used in thermal IPEM model

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal Conductivity (W/m-K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper</td>
<td>395</td>
</tr>
<tr>
<td>Aluminum</td>
<td>164</td>
</tr>
<tr>
<td>Ceramic AlN</td>
<td>150</td>
</tr>
<tr>
<td>Silicon</td>
<td>118</td>
</tr>
<tr>
<td>Ceramic Al₂O₃</td>
<td>26</td>
</tr>
<tr>
<td>Solder</td>
<td>51</td>
</tr>
<tr>
<td>Thermal Grease</td>
<td>1</td>
</tr>
<tr>
<td>Silicone Gel</td>
<td>0.2</td>
</tr>
<tr>
<td>Epoxy</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Table 3 Nominal values and measurement uncertainty of parameters used in sensitivity and uncertainty analyses

<table>
<thead>
<tr>
<th>Sensitivity Parameter, $\beta$</th>
<th>Location</th>
<th>Nominal Value, $\beta_{\text{Ni}}$</th>
<th>Measurement Uncertainty, $\sigma_{\text{ni}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Loss A</td>
<td>Innermost MOSFET</td>
<td>12 W</td>
<td>+3 W</td>
</tr>
<tr>
<td>Power Loss B</td>
<td>Outermost MOSFET</td>
<td>7 W</td>
<td>+3 W</td>
</tr>
<tr>
<td>Epoxy A</td>
<td>Between Silicon &amp; Ceramic Substrate</td>
<td>0.51 mm</td>
<td>±0.025 mm</td>
</tr>
<tr>
<td>Epoxy B</td>
<td>Between Gate Driver &amp; Ceramic Substrate</td>
<td>0.13 mm</td>
<td>±0.025 mm</td>
</tr>
<tr>
<td>Solder A</td>
<td>Between Silicon &amp; DBC Copper Trace</td>
<td>0.13 mm</td>
<td>±0.025 mm</td>
</tr>
<tr>
<td>Solder B</td>
<td>Between DBC Copper Base &amp; HS</td>
<td>0.13 mm</td>
<td>±0.025 mm</td>
</tr>
<tr>
<td>Thermal Grease</td>
<td>Between Heat Spreader (HS) &amp; Heat Sink</td>
<td>0.13 mm</td>
<td>±0.025 mm</td>
</tr>
</tbody>
</table>
$$X_j^+ = \frac{\delta T^+_j}{\delta \beta^+_i} = \frac{\Delta T^+_j}{\Delta \beta^+_i}$$

(1)

where $\Delta \beta^+_i$ is difference of the dimensionless perturbed parameter, defined as

$$\Delta \beta^+_i = \frac{\delta \beta^+_i}{\beta^+_i} = \frac{\beta^+_i - \beta_N}{\beta_N}$$

(2)

where $\beta_N$ is the nominal parameter value, and $\beta^+_i$ is the perturbed value. Thus, for a 1 percent variation in the nominal parameter value

$$\frac{\beta^+_i - \beta_N}{\beta_N} = \frac{(\beta_N + 0.01 \cdot \beta_N) - \beta_N}{\beta_N} = 0.01$$

(3)

That is, $\Delta \beta^+_i$ represents a 1 percent variation in the nominal parameter value, $\beta_N$. The nominal values used are also shown in Table 3.

The nondimensional temperature, $\Delta T^+$, is defined by

$$\Delta T^+ = \frac{T_N(\beta_N) - T_S(\beta_N)}{T_N(\beta_N) - T_\infty}$$

(4)

where $T_\infty$ is the ambient temperature, and $T_N(\beta_N)$ and $T_S(\beta_N)$ are the respective predicted temperatures for each parameter using $\beta_N$ and $\beta^+_i$. Note that $T_N(\beta_N)$ is also referred to as the nominal temperature.

The predictive uncertainties for each input parameter, $\sigma_{P_i}$, were then determined from the sensitivities and measurement uncertainties, $\sigma_{M_i}$, as follows [8]:

$$\sigma_{P_i} = X_i^+ \cdot \sigma_{M_i}$$

(5)

where $X_i^+$ is the sensitivity coefficient defined in Eq. (1). A dimensionless predictive sensitivity-uncertainty, $\sigma_{P_i}^+$, was then defined by

$$\sigma_{P_i}^+ = \frac{\sigma_{P_i}}{\beta_N}$$

(6)

where $\sigma_{P_i}$ is the predicted uncertainties for each input parameter and $\beta_N$ is the nominal parameter value. Finally, the overall uncertainty for the $j$th output variable, $\sigma_j$, was then defined as

$$\sigma_j = \sqrt{\sum_{i=1}^{Np} (\sigma_{P_i}^+)^2} = \sqrt{\sum_{i=1}^{Np} (X_i^+ \cdot \sigma_{M_i})^2}$$

(7)

where $Np$ is the number of critical input parameters.

**Results and Discussion**

**Results of the Electrical Analysis.** A summary of the results from the electrical analysis is provided here; details can be found in [6]. As a result of the parasitic inductance and capacitance analyses, a number of new layouts were proposed to reduce the geometric footprint of the module and improve electrical performance. The best of these resulted in Design B, and included a substantial reduction (by a factor of 3) in the copper trace area and a 4 percent reduction in the geometric footprint, as shown in Fig. 4. In addition, a bus capacitor was added to reduce the voltage overshoot of the device during switching periods.

The effects of the smaller copper trace area and the DBC ceramic substrate thickness on the electrical performance were then evaluated. Both reducing the trace area and increasing the ceramic layer thickness were found to substantially increase electrical performance, while the choice of material (AlN or Al₂O₃) had only a moderate effect. Hence, since thermal resistance increases with thickness, a trade-off was expected between electrical and thermal performance.

**Results From the Thermal Analysis.** A thermal analysis was first conducted on Design A and Design B to determine the overall temperature distributions and the peak temperatures, as shown in Fig. 5 and Table 4. The maximum temperature in both cases was located at the outer MOSFET. Design B resulted in a maximum temperature increase of almost 4°C and an overall average increase of almost 3°C over Design A. Hence, although the reduction in the size of the footprint and the copper trace area in Design B increased electrical performance as noted previously, it decreased thermal performance.

Thus, the second phase of the thermal analysis involved a parametric study to identify critical factors to improve the thermal performance of Design B. Eight cases based on Design B were studied, as shown in Table 4. The maximum temperatures in the MOSFETs and the gate driver and the overall average temperature are provided for each case: all predicted satisfactory operation under the 125°C temperature limit with the inlet air temperature of 50°C, although some provided cooler device temperatures than others as discussed below. Nonetheless, we seek to provide the best operating conditions in this effort. Therefore, the thermal results discussed in the paper are compared relatively to Design A as we illustrate the integrated design methodology. The maximum MOSFET temperature difference between the cases under consideration and Design A is shown in Fig. 6.

The DBC ceramic layer was first investigated. The effect of the ceramic material was moderate: The use of AlN (Case 1) instead of Al₂O₃ reduced the junction temperature by only 1.5°C, despite the large change in thermal conductivity shown in Table 2. This is
due to its relatively low contribution to the overall thermal resistance of the IPEM. On the other hand, the interface materials within the module are the most significant contributor to the overall thermal resistance. To take advantage of the high thermal conductivity of the AlN, the interface thermal resistance between the MOSFETs and the ceramic needs to be reduced.

The thickness of the ceramic was investigated next. A study of both the electrical and thermal responses due to different DBC ceramic thicknesses was implemented using the integrated software tools [12]. These tools allowed for the automated implementation of both the electrical and thermal parametric studies, thus, significantly reducing analysis time. The thickness of the layer was varied between 0.2 and 1.2 mm. The results are shown in Fig. 7, and also in Table 4 for 0.38 mm (Case 2) and 1.02 mm (Case 3). From Fig. 7, the common mode current decreases and the MOSFET temperature increases as the DBC ceramic thickness increases, although the effect on the electrical performance is significantly greater than that for the thermal performance. Therefore, the best selection of the DBC ceramic thickness was based on the trade-offs between electrical and thermal performance as well as commercially available thicknesses.

The effect of adding a copper heat spreader on the module was then analyzed, as shown by Cases 4 – 6 in Table 4 and Fig. 6. The addition of the heat spreader was most significant, as the maximum MOSFET and average temperatures dropped up to 7°C below Design B values. Note that the lower Cu layer was soldered onto the heat spreader, and then the heat spreader was placed on the heat sink with thermal grease. In the case without the heat spreader, thermal grease was used between the module and the heat sink. The effect of the thickness of the heat spreader was moderate as shown in Fig. 8. The MOSFET temperature increased 1°C as the thickness increased from 1 to 5 mm, while the average and gate temperature increased 2°C. These results agree with those presented by the Toshiba Corporation [4]. The temperature rise here is small since the material was copper. As a result, the heat spreader hindered the heat transfer slightly due to the added resistance layer, but it promoted heat transfer even more by pro-

| Table 4 Summary of results from the thermal simulations and the parametric study |
|----------------------------------|----------------|-----------------|----------------|-----------------|--------------------|--------------------|
| IPEM Model | IPEM Size (mm³) | Ceramic Mat’ls | DBC Ceramic Thickness (mm) | Heat Spreader (HS) Thickness (mm) | Max. MOSFET Temp. (°C) | Max. Gate Temp. (°C) | Avg. Module Temp. (°C) |
| Base Models |                |                |                              |                              |                    |                    |                      |
| Design A   | 26.9 x 30.0    | Al₂O₃          | 0.635                        | NA                           | 92.2               | 87.4               | 88.1                 |
| Design B   | 28.5 x 27.3    | Al₂O₃          | 0.635                        | NA                           | 95.9               | 93.2               | 90.7                 |
| Design B Modifications |            |                |                              |                              |                    |                    |                      |
| Case 2 (AlN) | 28.5 x 27.3    | AlN            | 0.38                         | NA                           | 94.4               | 92.2               | 90.1                 |
| Case 3 (1.02 mm DBC) | 28.5 x 27.3 | Al₂O₃          | 1.02                         | NA                           | 96.0               | 93.1               | 90.6                 |
| Case 4 (1 mm HS) | 28.5 x 27.3  | Al₂O₃          | 0.635                        | 1                            | 88.7               | 87.7               | 84.2                 |
| Case 5 (3 mm HS) | 28.5 x 27.3  | Al₂O₃          | 0.635                        | 3                            | 89.3               | 88.7               | 85.8                 |
| Case 6 (5 mm HS) | 28.5 x 27.3  | Al₂O₃          | 0.635                        | 5                            | 89.7               | 89.6               | 86.2                 |
| Case 7 (AlN+ 5 mm HS) | 28.5 x 27.3 | AlN            | 0.635                        | 5                            | 88.3               | 88.4               | 85.6                 |
| Case 8 (5 mm HS +Centered) | 28.5 x 27.3 | Al₂O₃          | 0.635                        | 5                            | 89.7               | 89.8               | 86.5                 |

Fig. 6 Maximum MOSFET temperature for Design B and 8 cases from parametric study in comparison to Design A results shown as baseline

Fig. 7 Trade-offs between electrical and thermal performance for different DBC ceramic thicknesses
viding a large conductive surface to dissipate heat. Case 7 shows the effect of the material choice for the ceramic layer with the 5 mm heat spreader. Although this case provided the best thermal performance, the improvement was moderate, as the AlN ceramic resulted in a 1.4°C decrease in the MOSFET temperature compared to Case 6 (Al2O3 ceramic).

Case 8 evolved through an analysis of Case 6. In looking at the temperature distribution on the heat spreader in Case 6, it was evident that the heat flow was asymmetric, and this prompted a modification to increase the heat spreader’s effectiveness. The heat spreader was centered under both MOSFETs, resulting in Case 8. Although the resulting temperature distribution is more symmetrical, the MOSFET temperature was virtually unchanged and the gate driver temperature increased slightly. However, both Cases 6 and 8 are significantly lower than Design B in Fig. 5(b). The temperature distribution on the heat spreader for Case 8 [Fig. 9(d)] revealed that although it appeared that the heat was being effectively distributed from the MOSFETs, there was little evidence that the same was true for the gate driver. Thus, even though power loss of the gate driver was only 1 W, it became the limiting factor in the thermal analysis, indicating a need for future detailed analyses of the gate driver.

Sensitivity and Uncertainty Analysis. In any modeling analyses, it is important to understand the uncertainty in the predicted temperatures. The Design B IPEM with a 5 mm thick heat spreader (Case 5) was chosen as the model for all of the uncertainty analyses. Sensitivity coefficients, Xij, were calculated using Eq. (1) for each of the critical input parameters as they affect each of the output variables; results are shown in Fig. 10. The most sensitive parameter is the thickness of Solder B, which is between the DBC copper layer and the heat spreader, followed by power loss A (12 W). The sensitivity of the solder thickness at the chip temperature is well over three times higher than that of the other parameters. A small variation in the solder thickness can result in larger temperature rise of the chip compared to the other parameters because most of the heat in the IPEM is removed through the bottom surface of the IPEM to the heat spreader and then the heat sink. On the other hand, the variation in the other parameters is considered to be insignificant in all cases. As a result, an accurate input of the thickness of Solder B is crucial for predicting a reliable chip temperature.

The predicted dimensionless sensitivity-uncertainty of each input parameter was then calculated from Eq. (6) using the sensitivities in Fig. 10 and the measurement uncertainties in Table 3. The results are shown in Fig. 11. Again, the thickness of Solder B, between the DBC copper layer and the heat spreader, contributed the highest uncertainty in the IPEM model.

The overall uncertainty was then calculated using Eq. (7) for each of the critical output variables, as shown in Fig. 12. The result shows that the junction temperature has the most uncertainty followed by the average temperature of IPEM. The minimum heat sink temperature has the least uncertainty among the four investigated temperatures. Based on the results we obtained, we can characterize the uncertainty associated with the thermal model.

Thus, from this analysis, the predicted chip junction temperature has the highest uncertainty at 8°C. Most importantly, this analysis emphasizes the importance of developing methodologies to accurately estimate power losses and interface conditions.

Design Selection. In selecting the best design, we realize that
there are trade-offs between the electrical, thermal, and practical considerations. With regards to the choice of the ceramic layer, we can see from Fig. 7 that the 0.64 mm thick DBC ceramic is the best selection based on the trade-off between electrical and thermal performance. In addition, Fig. 13 shows the cost of DBC ceramic at different thickness for different materials and Table 5 summarizes the tradeoff between the electrical performance and the cost of the DBC. The cost of a 1.02 mm thick DBC ceramic is 14 percent more expensive than a 0.64 mm thick DBC ceramic while the electrical performance at 0.64 mm thick DBC ceramic is 46 percent better. Similarly, the electrical performance at 0.38 mm thick DBC ceramic is 37 percent better than 0.64 mm thick DBC ceramic. However, the cost of a 0.38 mm thick DBC ceramic is 48 percent more expensive than a 0.64 mm thick DBC ceramic. Thus, based on this trade-off and cost considerations, we selected the optimum thickness at 0.64 mm. In either case, the AlN ceramic material proved to be beneficial, but was not chosen due to its comparably high cost illustrated in Fig. 13 making the selection of AlN as the ceramic material impractical at this moment since our goal is to achieve a low cost and reliable IPEM.

Although all the temperatures were well below the 125°C maximum limit, our effort aims to demonstrate the methodology in obtaining the lowest temperature. Table 4 shows that the thermal performance of the IPEM is better for the cases with heat spreader compared to the cases without heat spreader. Therefore, it is recommended to have the heat spreader to ensure the optimal thermal performance of the IPEM as well as the long term reliability. From Table 4 and Fig. 6, a 1 mm thick copper heat spreader would provide the best thermal performance. However, structural stability is an important factor too. Because of this and since the loss in thermal performance due to the increased thickness of the heat spreader was small, a 3 mm heat spreader was selected for the final design. Thus, the final design—Design C—consisted of the following modifications to design B: a 0.64 mm Al₂O₃ DBC ceramic layer with a 3 mm heat spreader, as shown in Table 6.

Summary and Conclusions

A two-step integrated design strategy was developed and implemented to improve the thermal and electrical performance of an IPEM design. The original design, Design A, consisted of (1) an IPEM module with a 26.9 mm×30.0 mm footprint and an almost equivalent copper trace area, (2) a 0.64 mm Al₂O₃ ceramic substrate layer, and (3) no heat spreader. The final design, named Design C, consisted of (1) an IPEM module with a 4 percent and 30 percent reduction in the footprint and copper trace, respectively, and an added bus capacitor, (2) a 0.635 mm Al₂O₃ ceramic substrate layer, and (3) a 3 mm heat spreader.

From the electrical perspective, a bus capacitor was added to reduce the voltage overshoot of semiconductor device, and the reduction in copper trace area reduced the O-to-Ground capacitance to 30 percent of the Design A value.

The thermal analysis demonstrated that the choice of material and thickness of the DBC ceramic layer had only a moderate effect on the thermal performance compared to the higher thermal resistance contributed by the interface materials within the IPEM. However, if the costs could be justified, AlN would be a better ceramic material choice than the Al₂O₃, due to its higher thermal conductivity. The addition of the copper heat spreader had a significant effect on the thermal performance, as the presence of a 1 mm layer decreased the maximum temperature of Design B by 7°C. The choice of a 3 mm layer was due to structural consider-
lations. In addition, it was found that the heat dissipation from the gate driver is poor, and should be examined more carefully in the future. It should be emphasized that, due to the complexity of the multsource interactions, these observations could have not been easily visualized without the detailed three-dimensional (3D) thermal analysis.

In addition, the implementation of the integrated software tool has effectively performed multidisciplinary analyses in a systematic way. The feasibility of the approach is illustrated through the integrated analysis used for the parametric study of the trade-offs between the EMI and the thermal performance due to different DBC ceramic thicknesses.

The sensitivity analysis demonstrated the importance of accuracy in the input parameters, particularly for the most sensitive parameters which were Solder B, Power Loss A, and Power Loss B for this study. They noticeably affected the overall uncertainty of the predicted output temperatures with the highest uncertainty being 8°C for the junction temperature. However, even with this uncertainty taken into account, all predicted temperatures were well below the 125°C maximum limit. Again, our focus was to optimize and reduce the internal thermal resistance of the module under the worst operating conditions. Since the purpose of this paper is to demonstrate the integrated design methodology, the uncertainties in the material properties were not considered in the uncertainty analysis at this time. However, the same methodology can also be used to investigate the uncertainties in the material properties.

Thus, in conclusion, the two-step integrated design strategy was successfully used to redesign the existing Design A IPEM. The final design, Design C, provided a 70 percent reduction in the common mode current, a 4 percent reduction in the size of the geometric footprint, and a 3°C reduction in the maximum temperature over Design A, thus providing an increase in the overall performance. More importantly, the integrated software tool demonstrates a feasible and systematic way of performing multidisciplinary analyses. While only electrical and thermal performances were described in this paper, the integrated design strategy can also be applied to include mechanical analysis and cost analysis.

Acknowledgment

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Nomenclature

\[ N_p = \text{Total number of critical input parameters} \]
\[ t = \text{Time} \]
\[ T = \text{Temperature} \]
\[ X_{ij} = \text{Sensitivity coefficient of output variable } j \text{ to input parameter } i \]

\[ \beta = \text{Input parameter} \]
\[ \sigma = \text{Output uncertainty} \]

Superscripts

\[ M = \text{Measurement} \]
\[ N = \text{Nominal value} \]
\[ P = \text{Predictive} \]
\[ S = \text{Sensitivity or perturbed value} \]
\[ + = \text{Dimensionless} \]
\[ \approx = \text{Ambient} \]

Acronyms

\begin{itemize}
  \item AIN = Aluminum Nitride
  \item Al₂O₃ = Aluminum Oxide
  \item CFD = Computational Fluid Dynamic
  \item DBC = Direct Bonded Copper
  \item EMI = Electromagnetic Interference
  \item IGBT = Insulated Gate Bipolar Transistor
  \item IPEM = Integrated Power Electronics Module
  \item MCM = Multi Chip Module
  \item MOSFET = Metal Oxide Semiconductor Field Effect Transistor
\end{itemize}

References

[9] I-DEAS Master Series, 2000, version 8, SDRC, Milford, OH.